What is claimed is:

1) A method of fabricating a semiconductor device comprising the steps:

forming a pre-amorphized implant layer in between shallow trench isolation regions and adjacent to gate electrode structure on a semiconductor substrate;

performing ion implantation in said pre-amorphized implant layer to form source/drain extension regions; and

performing a sequential dual step annealing of said source/drain extension regions.

2) The method of fabricating a semiconductor device according to claim **1**, wherein said pre-amorphitization implantation is done with ions comprising Ge^+ or Si^+.

3) The method of fabricating a semiconductor device according to claim **2**, wherein said Ge^+ or Si^+ ion implant ion energy is approximately between 1 keV and 20 keV and the dose is approxi-mately between 1E14 and 1E16 ions/cm^2.

4) The method of fabricating a semiconductor device according to claim **1**, wherein said SDE implant is done with B^+ ions.

5) The method of fabricating a semiconductor device according to claim **4**, wherein said B^+ ion implant energy is approximately between 0.2 keV and 0.7 keV and the dose is approximately between 5E14 and 1E16 ions/cm^2.

6) The method of fabricating a semiconductor device according to claim **1**, wherein said sequential dual step anneal comprises low temperature anneal followed by rapid thermal anneal.

7) The method of fabricating a semiconductor device according to claim **6**, wherein said low temperature annealing is done with laser irradiation.

8) The method of fabricating a semiconductor device according to claim **7**, wherein said laser irradiation is done using a multiple-pulsed 248 nm KrF excimer laser beam.

9) The method of fabricating a semiconductor device according to claim **8**, wherein said laser beam has a fluence of approximately between 0.1 J/cm^2 and 0.4 J/cm^2, pulse duration of approximately between 10 nsec and 40 nsec, and a repetition rate of 1 – 1000 pulses.

10) The method of fabricating a semiconductor device according to claim **6**, wherein said rapid thermal anneal is done at approximately between 800 °C and 1200 °C for a duration of approximately between 0 sec and 60 sec.

11) A method of fabricating a MOSFET device with shallow source/drain extension junctions comprising the steps:

forming a pre-amorphized Ge^+ or Si^+ implant layer in between shallow trench isolation regions and adjacent to gate electrode structure on a silicon substrate;

performing B^+ion implantation in said pre-amorphized implant layer to form source/drain extension regions; and

performing a sequential dual step annealing of said source/drain extension regions comprising low temperature laser anneal and rapid thermal anneal..

12) The method of fabricating a MOSFET device with shallow source/drain extension junctions according to claim **11**, wherein said Ge^+ or Si^+ ion implant ion energy is approximately between 1 keV and 20 keV and the dose is approximately between 1E14 and 1E16 ions/cm^2.

13) The method of fabricating a MOSFET device with shallow source/drain extension junctions according to claim **11**, wherein said B^+ ion implant energy is approximately between 0.2 keV and 0.7 keV and the dose is approximately between 5E14 and 1E16 ions/cm^2.

14) The method of fabricating a MOSFET device with shallow source/drain extension junctions according to claim **11**, wherein said low temperature laser anneal is done using a multiple-pulsed 248 nm KrF excimer laser beam.

15) The method of fabricating a MOSFET device with shallow source/drain extension junctions according to claim **14**, wherein said multiple-pulsed laser beam has a fluence of approximately between 0.1 J/cm^2 and 0.4 J/cm^2, pulse duration of approximately between 10 nsec and 40 nsec, and a repetition rate of 1 – 1000 pulses.

16) The method of fabricating a MOSFET device with shallow source/drain extension junctions according to claim **11**, wherein said rapid thermal anneal is done at approximately between 800 °C and 1200 °C for a duration of approximately between 0 sec and 60 sec.

17) A method of forming shallow source/drain extension junctions in a MOSFET device, comprising the steeps:

performing B^+ion implantation in a pre-amorphized implant layer to form source/drain extension regions on a silicon substrate; and

performing a sequential dual step annealing of said source/drain extension regions comprising low temperature laser anneal and rapid thermal anneal.

18) The method of forming shallow source/drain extension junctions in a MOSFET device according to claim **17**, wherein said B^+ ion implant energy is approximately between 0.2 keV and 0.7 keV and the dose is approximately between 5E14 and 1E16 ions/cm^2.

19) The method of forming shallow source/drain extension junctions in a MOSFET device according to claim **17**, wherein said low temperature laser anneal is done using a multiple-pulsed 248 nm KrF excimer laser beam.

20) The method of forming shallow source/drain extension junctions in a MOSFET device according to claim **19**, wherein said multiple-pulsed laser beam has a fluence of approximately between 0.1 J/cm^2 and 0.4 J/cm^2, pulse duration of approximately between 10 nsec and 40 nsec, and a repetition rate of 1 – 1000 pulses.

21) The method of forming shallow source/drain extension junctions in a MOSFET device according to claim **17**, wherein said rapid thermal anneal is done at approximately between 800 °C and 1200 °C for a duration of approximately between 0 sec and 60 sec.

22) A method of forming a MOSFET device with shallow source/drain extension junctions, comprising the steps:

forming shallow trench isolation regions on a silicon substrate;

forming the gate stack in between said shallow trench isolation regions;

removing the sidewall spacers from around said gate stack;

forming a pre-amorphized Ge^+ or Si^+ implant layer in silicon, between shallow trench isolation regions and adjacent to gate electrode structure;

performing B^+ion implantation in said pre-amorphized implant layer to form source/drain extension regions; and

performing a sequential dual step annealing of said source/drain extension regions comprising low temperature multiple-pulsed laser anneal and rapid thermal anneal..

23) The method of forming a MOSFET device with shallow source/drain extension junctions according to claim **22**, wherein said Ge^+ or Si^+ ion implant ion energy is approximately between 1 keV and 20 keV and dose is approximately between 1E14 and 1E16 ions/cm^2.

24) The method of forming a MOSFET device with shallow source/drain extension junctions according to claim **22**, wherein said B^+ ion implant energy is approximately between 0.2 keV and 0.7 keV and the dose is approximately between 5E14 and 1E16 ions/cm^2.

25) The method of forming a MOSFET device with shallow source/drain extension junctions according to claim **22**, wherein said multiple-pulsed laser beam is a 248 nm KrF excimer laser with a fluence of approximately between 0.1 J/cm^2 and 0.4 J/cm^2, pulse duration

of approximately between 10 nsec and 40 nsec, and a repetition rate of 1 – 1000 pulses.

26) The method of forming a MOSFET device with shallow source/drain extension junctions according to claim **22**, wherein said rapid thermal anneal is done at approximately between 800 °C and 1200 °C for a duration of approximately between 0 sec and 60 sec.